

1      **CLAIMS:**

2      1. A method of forming a semiconductor construction,  
3      comprising:

4              forming a first substrate comprising silicon-containing structures  
5      separated from one another by an insulative material; the silicon-  
6      containing structures defining an upper surface;

7              forming a second semiconductor substrate comprising a  
8      monocristalline material having a damage region therein;

9              bonding the second semiconductor substrate to the silicon-  
10     containing structures at the upper surface; and

11              cleaving the monocristalline material along the damage region.

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13      2. The method of claim 1 wherein the cleaving leaves a rough  
14     upper surface of the monocristalline material over the silicon-containing  
15     structures; and further comprising, after the cleaving, smoothing the  
16     upper surface of the monocristalline material.

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18      3. The method of claim 1 wherein the silicon-containing  
19     structures comprise conductively-doped silicon.

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21      4. The method of claim 1 wherein the silicon-containing  
22     structures comprise amorphous silicon.

1           5. The method of claim 1 wherein the silicon-containing  
2           structures comprise polycrystalline silicon.

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4           6. The method of claim 1 wherein the silicon-containing  
5           structures comprise monocrystalline silicon.

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7           7. A method of forming a semiconductor construction,  
8           comprising:

9           forming a first semiconductor substrate comprising a first  
10          monocrystalline base and having a first transistor supported on the first  
11          monocrystalline base; the first transistor having source/drain regions  
12          associated therewith; the first substrate also having an insulative material  
13          formed over the base and silicon-containing plugs extending through the  
14          insulative material and to the source/drain regions; the silicon-containing  
15          plugs being separated from one another by the insulative material and  
16          defining a planarized upper surface above the first monocrystalline base;

17           providing a second semiconductor substrate comprising a second  
18          monocrystalline base and bonding the second semiconductor substrate to  
19          the silicon-containing plugs at the planarized upper surface above the  
20          first monocrystalline base; and

21           forming a second transistor supported over the second substrate.

1           8. The method of claim 7 wherein one of the first and second  
2           transistors is a PMOS transistor and wherein the other of the first and  
3           second transistors is an NMOS transistor.

4           5           9. The method of claim 7 wherein the second transistor  
6           comprises source/drain regions which extend entirely through the second  
7           monocrystalline base.

8           9           10. The method of claim 7 wherein the second transistor  
10          comprises source/drain regions which extend only partially through the  
11          second monocrystalline base.

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1           11. A method of forming a semiconductor construction,  
2 comprising:

3           forming a first semiconductor substrate comprising a first  
4 monocrystalline base and silicon-containing structures above the base, at  
5 least some of the silicon-containing structures being separated from one  
6 another by an insulative material; the silicon-containing structures and  
7 insulative material together defining a planarized upper surface above  
8 the first monocrystalline base;

9           forming a second semiconductor substrate comprising a second  
10 monocrystalline base and having a damage region formed within the  
11 second monocrystalline base;

12           bonding the second semiconductor substrate to the silicon-  
13 containing structures at the planarized upper surface above the first  
14 monocrystalline base; and

15           cleaving the second monocrystalline base along the damage region.

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17           12. The method of claim 11 the first and second monocrystalline  
18 bases comprise monocrystalline silicon.

1       13. The method of claim 11 wherein some of the silicon-  
2       containing structures have no function except to bond to the second  
3       semiconductor substrate; and wherein others of the silicon-containing  
4       structures have additional functions besides bonding to the second  
5       semiconductor substrate.

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7       14. The method of claim 11 wherein the second monocrystalline  
8       base is bonded to the silicon-containing structures.

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10      15. The method of claim 11 wherein the bonding the second  
11       semiconductor structure comprises bonding the second monocrystalline  
12       base to the silicon-containing structures, and bonding the second  
13       monocrystalline base to the insulative material at the planarized upper  
14       surface above the first monocrystalline base.

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16      16. The method of claim 11 wherein the damage region is  
17       formed by implanting hydrogen ions into the second monocrystalline  
18       base.

1           17. The method of claim 11 wherein the damage region is  
2           formed by implanting hydrogen ions into the second monocrystalline  
3           base, and wherein the cleaving comprise thermally treating the second  
4           monocrystalline base.

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6           18. The method of claim 11 wherein the only temperatures  
7           utilized for the bonding are less than or equal to about 700°C, and  
8           further comprising not exposing the first monocrystalline base to  
9           temperatures exceeding 700°C after the bonding.

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11           19. The method of claim 11 further comprising forming at least  
12           one doped silicon region extending through the second monocrystalline  
13           base and electrically contacting at least one of the silicon-containing  
14           structures.

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16           20. The method of claim 11 further comprising:  
17           forming at least one doped silicon region extending through the  
18           second monocrystalline base and electrically contacting at least one of  
19           the silicon-containing structures; and

20           forming at least one other doped silicon region within the second  
21           monocrystalline base, but which does not extend entirely through the  
22           second monocrystalline base.

1           21. A method of forming a semiconductor construction,  
2 comprising:  
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4           forming a first substrate comprising silicon-containing structures  
5 separated from one another by an insulative material; the silicon-  
6 containing structures defining an upper surface;

7           bonding a second semiconductor substrate to the silicon-containing  
8 structures at the upper surface; the second semiconductor substrate  
9 comprising a monocrystalline material which is bonded to the silicon-  
10 containing structures; and

11           forming at least one doped silicon region extending through the  
12 monocrystalline material and electrically contacting at least one of the  
13 silicon-containing structures.

14           22. The method of claim 21 wherein the forming the at least  
15 one doped silicon region comprises implanting dopant into the  
16 monocrystalline material.

17           23. The method of claim 21 further comprising forming at least  
18 one insulative region extending at least partially into the monocrystalline  
19 material.

1           24. The method of claim 21 further comprising forming at least  
2           one insulative region extending through the monocrystalline material.

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4           25. The method of claim 24 wherein the forming the at least  
5           one insulative region comprises:

6           forming an opening through the monocrystalline material; and  
7           filling the opening with an insulative material.

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9           26. The method of claim 21 wherein the forming the at least  
10          one doped silicon region comprises:

11          forming an opening through the monocrystalline material; and  
12          filling the opening with a doped silicon material.

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14          27. The method of claim 26 wherein the doped silicon material  
15          comprises doped amorphous silicon.

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17          28. The method of claim 26 wherein the doped silicon material  
18          comprises doped polycrystalline silicon.

1           29. The method of claim 21 further comprising forming at least  
2       one second doped silicon region within the second monocrystalline base  
3       and which does not extend entirely through the second monocrystalline  
4       base.

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6           30. The method of claim 29 wherein the forming the at least  
7       one doped silicon region comprises:

8           forming an opening through the monocrystalline material; and  
9           filling the opening with a doped silicon material.

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11           31. The method of claim 30 wherein the doped silicon material  
12       comprises doped amorphous silicon.

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14           32. The method of claim 30 wherein the doped silicon material  
15       comprises doped polycrystalline silicon.

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1           33. A semiconductor construction, comprising:

2           a first substrate comprising silicon-containing structures separated  
3           from one another by an insulative material; the silicon-containing  
4           structures defining an upper surface; and

5           a second semiconductor substrate comprising a monocrystalline  
6           material bonded over the silicon-containing structures at the upper  
7           surface.

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9           34. The construction of claim 33 further comprising one of  
10          either a PMOS or NMOS transistor having a gate between the first and  
11          second substrates; and the other of a PMOS or NMOS transistor having  
12          a gate over the second substrate.

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14          35. The construction of claim 33 further comprising only one  
15          type of PMOS type or NMOS type transistors having a gate between  
16          the first and second substrates; and the other type PMOS type and  
17          NMOS type transistors having a gate over the second substrate.

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19          36. The construction of claim 33 further comprising only one  
20          type of PMOS type or NMOS type transistors having a gate between  
21          the first and second substrates; and both types of PMOS type and  
22          NMOS type transistors having gates over the second substrate.

1           37. The construction of claim 33 further comprising both types  
2 of PMOS type and NMOS type transistors having gates between the first  
3 and second substrates; and only one type of the PMOS type and NMOS  
4 type transistors having a gate over the second substrate.

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6           38. The construction of claim 33 wherein the monocrystalline  
7 material of the second semiconductor substrate is monocrystalline silicon.

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9           39. The construction of claim 33 wherein the silicon-containing  
10 structures comprise conductively-doped silicon.

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12          40. The construction of claim 33 wherein the silicon-containing  
13 structures comprise amorphous silicon.

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15          41. The construction of claim 33 wherein the silicon-containing  
16 structures comprise polycrystalline silicon.

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18          42. The construction of claim 33 wherein the silicon-containing  
19 structures comprise monocrystalline silicon.

1           43. A semiconductor construction, comprising:

2           a first semiconductor substrate comprising a first monocrystalline  
3           base and silicon-containing structures above the base, at least some of  
4           the silicon-containing structures being separated from one another by an  
5           insulative material; the silicon-containing structures and insulative  
6           material together defining an upper surface above the first  
7           monocrystalline base; and

8           a second semiconductor substrate comprising a second  
9           monocrystalline base bonded to the silicon-containing structures at the  
10           upper surface above the first monocrystalline base.

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12           44. The construction of claim 40 the first and second  
13           monocrystalline bases comprise monocrystalline silicon.

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15           45. The construction of claim 40 wherein the second  
16           monocrystalline base is bonded to the insulative material at the upper  
17           surface above the first monocrystalline base.

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19           46. The construction of claim 40 further comprising at least one  
20           electrically insulative region extending through the second  
21           monocrystalline base.

1           47. The construction of claim 40 further comprising at least one  
2           doped silicon region extending through the second monocrystalline base  
3           and electrically contacting at least one of the silicon-containing  
4           structures.

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6           48. The construction of claim 40 further comprising:  
7           at least one doped silicon region extending through the second  
8           monocrystalline base and electrically contacting at least one of the  
9           silicon-containing structures; and  
10           at least one insulative region extending through the second  
11           monocrystalline base.

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13           49. The construction of claim 40 further comprising:  
14           at least one doped silicon region extending through the second  
15           monocrystalline base and electrically contacting at least one of the  
16           silicon-containing structures; and  
17           at least one doped silicon region within the second monocrystalline  
18           base, but which does not extend entirely through the second  
19           monocrystalline base.